AMENDMENT TO THE CLAIMS

1-19 (Cancelled).

20. (Currently Amended) A method of manufacturing of a multilayer semiconductor structure comprising a high resistivity silicon substrate with a resistivity higher than 3 kΩ.cm, an intermediate layer, ~~an active semiconductor layer and~~ an insulating layer and an active semiconductor layer, ~~in between the silicon substrate and the active semiconductor layer,~~ wherein the method comprises:

forming the intermediate layer by depositing an amorphous silicon layer and then crystallising the amorphous silicon layer to form a polycrystalline layer which is located between the high resistivity silicon substrate and the insulating layer in order to increase the charge trap density between the insulating layer and the high resistivity silicon substrate, thereby suppressing ohmic losses inside the high resistivity silicon substrate ~~suppressing ohmic losses inside the high resistivity silicon substrate by increasing charge trap density between the insulating layer and the silicon substrate~~.

21. (Currently Amended) [[A]] The method according to claim 20, wherein ~~increasing charge trap density comprises applying an intermediate layer in between the silicon substrate and the insulating layer,~~ the intermediate layer [[comprising]] comprises grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm~~, preferably smaller than 50 nm~~.

22. (Currently Amended) [[A]] The method according to claim 21, wherein the intermediate layer has a charge trap density of ~~at least $10^{11}/cm^2/eV$, preferably~~ at least $10^{12}/cm^2/eV$.

23. (Cancelled)

24. (Currently Amended) [[A]] The method according to claim 21, the intermediate layer having an RMS roughness, wherein the RMS roughness of the intermediate layer has an average value smaller than or equal to 0.5 nm.

25. (Cancelled)

26. (Currently Amended) [[A]] The method according to claim 20 [[25]], wherein crystallizing comprises any of thermal annealing or rapid thermal annealing (RTA) or laser crystallisation.

27. (Currently Amended) [[A]] The method according to claim 21, the method comprising bonding [[an]] the intermediate layer-covered high resistivity silicon substrate to an insulator-passivated semiconductor substrate.

28. (Currently Amended) [[A]] The method according to claim 27, the method comprising a surface oxidation of the intermediate layer prior to bonding the high resistivity silicon substrate to the insulator-passivated semiconductor substrate.

29. (Currently Amended) [[A]] The method according to claim 21, the method comprising providing an intermediate layer on an insulator-passivated semiconductor substrate, and bonding [[this]] the intermediate layer insulator-passivated semiconductor substrate to a high-resistivity silicon substrate.

30. (Currently Amended) [[A]] The method according to claim 21, wherein the intermediate layer has a layer thickness of ~~at least 100 nm, preferably~~ between 100 nm and 450 nm, ~~more preferred between 200 nm and 300 nm~~.

31. (Currently Amended) [[A]] The method according to claim 21, wherein the density of charge traps remains higher than or equal to $10^{11}/cm^2/eV$ ~~after a standard CMOS process is performed on the structure~~.

32. (Currently Amended) A multilayer structure comprising a high resistivity silicon substrate with a resistivity higher than 3 kΩ.cm, an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer, wherein the multilayer structure comprises an intermediate layer in between the high resistivity silicon substrate and the insulating layer, the intermediate layer being a re-crystallized polysilicon layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm~~, preferably smaller than 50 nm~~.

33. (Currently Amended) [[A]] The multilayer structure according to claim 32, wherein the intermediate layer has a trap density of at least $10^{11}/cm^2/eV$~~, preferably at least $10^{12}/cm^2/eV$~~.

34. (Currently Amended) [[A]] The multilayer structure according to claim 32, wherein the multilayer structure has an effective resistivity higher than 5 kΩ.cm~~, preferably higher than 10 kΩ.cm~~.

35. (Cancelled)

36. (Currently Amended) [[A]] The multilayer structure according to claim 32, wherein the intermediate layer has an RMS roughness with an average value smaller than or equal to 0.5 nm.

37. (Currently Amended) [[A]] The multilayer structure according to claim 32, wherein the active semiconductor layer is made from at least one of Si, Ge, Si_xGe_y, SiC, InP, GaAs or GaN.

38. (Currently Amended) [[A]] The multilayer structure according to claim 32, wherein the insulating layer is formed of at least one of an oxide, a nitride, Si_3N_4, a porous insulating material, a low-k insulating material, a high-k dielectric or a polymer.

39. (New) The method according to claim 32, wherein increasing charge trap density comprises applying an intermediate layer in between the silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 50 nm.

40. (New) The method according to claim 21, wherein the intermediate layer has a charge trap density of at least $10^{12}/cm^2/eV$.

41. (New) The method according to claim 21, wherein the intermediate layer has a layer thickness of between 200 nm and 300 nm.

42. (New) The method according to claim 21, wherein the intermediate layer has a layer thickness of at least 100 nm.

43. (New) The multilayer structure according to claim 32, wherein the intermediate layer has a trap density of at least $10^{12}/cm^2/eV$.

44. (New) The multilayer structure according to claim 32, wherein the multilayer structure has an effective resistivity higher than 10 kΩ.cm.

45. (New) A method of manufacturing of a multilayer semiconductor structure comprising a high resistivity silicon substrate with a resistivity higher than 3 kΩ.cm, and an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer, wherein the method comprises: introducing an intermediate layer between the silicon substrate and the insulating layer in order to increase the charge trap density between the insulating layer and the silicon substrate, thereby suppressing ohmic losses inside the high resistivity silicon substrate, the intermediate layer being formed in contact with the silicon substrate and the insulating layer, wherein applying the intermediate layer comprises applying any of an undoped or lightly doped silicon layer, an undoped polysilicon layer, a germanium layer, an undoped polygermanium layer or a poly-SiGe silicon carbide layer.

46. (New) The method according to claim 45, wherein increasing charge trap density comprises applying an intermediate layer in between the silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm.

47. (New) The method according to claim 45, wherein the intermediate layer has a charge trap density of at least $10^{12}/cm^2/eV$.

48. (New) The method according to claim 45, the intermediate layer having an RMS roughness, wherein the RMS roughness of the intermediate layer has an average value smaller than or equal to 0.5 nm.

49. (New) The method according to claim 45, wherein applying a polysilicon layer comprises depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer.

50. (New) The method according to claim 49, wherein crystallizing comprises any of thermal annealing or rapid thermal annealing (RTA) or laser crystallisation.

51. (New) The method according to claim 45, the method comprising bonding an intermediate layer-covered high resistivity silicon substrate to an insulator-passivated semiconductor substrate.

52. (New) The method according to claim 51, the method comprising a surface oxidation of the intermediate layer prior to bonding the high resistivity silicon substrate to the insulator-passivated semiconductor substrate.

53. (New) The method according to claim 45, the method comprising providing an intermediate layer on an insulator-passivated semiconductor substrate, and bonding the intermediate layer insulator-passivated semiconductor substrate to a high-resistivity silicon substrate.

54. (New) The method according to claim 45, wherein the intermediate layer has a layer thickness of between 100 nm and 450 nm.

55. (New) The method according to claim 45, wherein the density of charge traps remains higher than or equal to $10^{11}/cm^2/eV$.

56. (New) A multilayer structure comprising a high resistivity silicon substrate with a resistivity higher than 3 kΩ.cm, an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer,

wherein the multilayer structure comprises an intermediate layer in between the high resistivity silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm, the intermediate layer being in contact with the silicon substrate and the insulating layer, wherein the intermediate layer consists of any of an undoped or lightly doped silicon layer, an undoped polysilicon layer, a germanium layer, an undoped polygermanium layer or a poly-SiGe silicon carbide layer.

57. (New) The multilayer structure according to claim 56, wherein the intermediate layer has a trap density of at least $10^{11}/cm^2/eV$.

58. (New) The multilayer structure according to claim 56, wherein the multilayer structure has an effective resistivity higher than 5 kΩ.cm.

59. (New) The multilayer structure according to claim 56, wherein the intermediate layer has an RMS roughness with an average value smaller than or equal to 0.5 nm.

60. (New) The multilayer structure according to claim 56, wherein the active semiconductor layer is made from at least one of Si, Ge, Si_xGe_y, SiC, InP, GaAs or GaN.

61. (New) The multilayer structure according to claim 56, wherein the insulating layer is formed of at least one of an oxide, a nitride, Si_3N_4, a porous insulating material, a low-k insulating material, a high-k dielectric or a polymer.